WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a transistor on a semiconductor substrate; and

contact portions for connecting a lower layer and an upper layer arranged in plural lines.

2. A semiconductor device comprising:

a first transistor on a semiconductor substrate;

first contact portions for connecting a lower layer and an upper layer in the first transistor;

a second transistor on the semiconductor substrate; and

second contact portions for connecting a lower layer and an upper layer in the second transistor,

wherein numbers of the first contact portions and the second contact portions are different.

3. The semiconductor device according to claim 2, wherein the first contact portions are arranged in one line, and the second contact portions are arranged in plural lines.

4. The semiconductor device according to claim 2, wherein the second transistor further comprises:

a source/drain region formed to be adjacent to a gate electrode; and

a semiconductor region constituting a channel formed under the gate electrode.

5. The semiconductor device according to claim 4, wherein the second transistor further comprises a low concentration region of the same conductive type as the conductive type of the source/drain region, formed to connect to the source/drain region and to contact the semiconductor region under the gate electrode of the second transistor.

6. The semiconductor device according to claim 4, wherein the second transistor further comprises a low concentration region of the same conductive type as the conductive type of the source/drain region, formed being extended shallowly to the semiconductor region to connect to the source/drain region and to contact the semiconductor region under the gate electrode of the second transistor.

7. The semiconductor device according to claim 1, wherein the contact portions are provided for connecting to the source/drain region.

8. The semiconductor device according to claim 1, wherein the contact portions are provided for connecting to the lower layer wiring and the upper layer wiring.

9. The semiconductor device according to claim 1, wherein a conductive film is buried in the contact portions.

10. A semiconductor device comprising:

a low concentration opposite conductive type source/drain region formed in one conductive type semiconductor;

a high concentration opposite conductive type source/drain region formed in the low concentration opposite conductive type source/drain region;

a gate electrode formed on the semiconductor through gate oxide film;

a one conductive type semiconductor region formed under the gate electrode and constituting a channel placed between the source/drain region;

contact portions contacting arranged in plural lines; and

a source/drain electrode connected to the source/drain region through the contact portions.

11. A method of manufacturing a semiconductor device including transistors on a semiconductor substrate, the method comprising a step of forming contact portions for connecting a lower layer and an upper layer in plural lines.

12. A method of manufacturing a semiconductor device including a first transistor and a second transistor on a semiconductor substrate, the method comprising the steps of:

forming first contact portions for connecting a lower layer and an upper layer in the first transistor;

forming second contact portions for connecting a lower layer and an upper layer in the second transistor,

wherein numbers of the first contact portions and the second contact portions are different.

13. The method of manufacturing a semiconductor device according to claim 12, wherein the first contact portions are arranged in one line, and the second contact portions are arranged in plural lines.

14. The method of manufacturing a semiconductor device according to claim 11, wherein the contact portions are provided for connecting to the source/drain region.

15. The method of manufacturing a semiconductor device according to claim 11, wherein the contact portions are provided for connecting to the lower layer wiring and the upper layer wiring.

16. A method of manufacturing a semiconductor device including a gate electrode on a one conductive type semiconductor through gate oxide film, the method comprising the steps of:

forming a low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity in the semiconductor;

forming a low concentration opposite conductive type region connecting to the low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a high concentration opposite conductive type source/drain region in the low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a one conductive type body region dividing the opposite conductive type region under the gate electrode by ion-implanting one conductive type impurity; and

forming contact portions for connecting to the source/drain region in plural lines through an interlayer insulating film covering the gate electrode.

17. The method of manufacturing a semiconductor device according to claim 11, further comprising a step of burying a conductive film in the contact portions.

18. A semiconductor device not forming any via hole under a bump electrode provided at a pad portion.

19. A semiconductor device comprising:

an upper layer wiring;

a lower layer wiring;

a via hole connecting the upper layer wiring and the lower layer wiring; and

a bump electrode provided at a pad portion covering lower layer wiring,

wherein the via hole is formed at a region except under the bump electrode.

20. The semiconductor device according to claim 18,

wherein further comprising a lower layer wiring arranged under the bump electrode.

21. A semiconductor device comprising:

a gate electrode formed on a semiconductor substrate through gate oxide film;

a source/drain region formed so as to be adjacent to the gate electrode;

a semiconductor region formed under the gate electrode and constituting a channel;

a lower layer wiring connected to the source/drain region with contact;

a via hole formed in an interlayer insulating film covering the lower layer wiring and formed at a region except a bump electrode provided at a pad portion; and

an upper layer wiring connected to the lower layer wiring with contact through the via hole.

22. The semiconductor device according to claim 21, further comprising a low concentration region of the same conductivity type as the source/drain region formed under the gate electrode so as to connect to the source/drain region and to contact the semiconductor region.

23. A semiconductor device according to claim 21, further comprising a low concentration region of the same conductivity type as the source/drain region formed extending shallowly to surface layer of the semiconductor under the gate electrode so as to connect to the source/drain region and to contact the semiconductor region.

24. A method of manufacturing a semiconductor device not forming a via hole under a bump electrode constituted at a pad portion.

25. A method of manufacturing a semiconductor device connecting to an upper layer wiring with contact through a via hole formed interlayer insulating film covering a lower layer wiring, the method comprising the steps of:

forming in the interlayer insulating film so as to cover the lower layer wiring;

forming the upper layer wiring so as to contact the lower layer wiring through the via hole after forming the via hole at region except a pad forming portion of the interlayer insulating film; and

forming a bump electrode at a pad portion.

26. The method of manufacturing a semiconductor device according to claim 24, forming a lower layer wiring under the bump electrode.

27. A method of manufacturing a semiconductor device including a gate electrode on a one conductive type semiconductor through gate oxide film, the method comprising the steps of:

forming a low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity in the semiconductor;

forming a low concentration opposite conductive type region connecting to the low concentration opposite

conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a high concentration opposite conductive type source/drain region in the low concentration opposite conductive type source/drain region by ion-implanting opposite conductive type impurity;

forming a one conductive type body region dividing the opposite conductive type region under the gate electrode by ion-implanting one conductive type impurity;

forming a lower layer wiring connecting to the source/drain region with contact through interlayer insulating film covering the gate electrode;

forming a via hole at a region except a bump electrode provided at a pad portion of the interlayer insulating film after forming the interlayer insulating film to cover the lower layer wiring; and

forming an upper layer wiring connected to the lower layer wiring through the via hole.